ABSTRACT OF THE DISCLOSURE

A system and method for implementing an SMBus/I^2C interface in a computer connectable to a network. The system includes a plurality of devices communicably coupled to an SMBus. The system operates at a first clock rate when the system is awake, and at a second clock rate less than the first clock rate when the system is sleeping. At least when the system is sleeping, a first device stores data transferred via the SMBus in a register, and a second device drives the clock line of the SMBus to a low logic level while the data is stored in the register of the first device. Upon completion of the data transfer operation, the first device clears the data from the register, and the second device releases the clock line to allow it to be pulled-up by pull-up circuitry connected to the SMBus.

226798

ATTORNEY DOCKET NO. SYNER-164XX
WEINGARTEN, SCHURGIN,
GAGNEBIN & HAYES, LLP
TEL. (617) 542-2290
FAX. (617) 451-0313